Table 1 PCAMAP History

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| PCA­MAP REV | PCA NUMBER AND REVISION  (73-BBBB-VV\_RR) | ECO/CUP | DATE | HW VER. | ENGINEER | REASON/PURPOSE OF CHANGE |
| -A0 | 73-102931-02\_A0 | EA600445 | 10/28/2022 | 1.0 | Kuouyang | SD1 ASIC change from 08-1199-01 to 08-1199-02 |
| -A0 | 73-102931-03\_A0 | EA600756 | 12/20/2022 | 1.0 | Mikchang | Release alternate circuit BOM to production |
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# Purpose

* 1. This document is to be used to assemble Superfuzz 73-102931-03.
  2. This document provides electronic identification and programming instructions.
  3. This document defines the instructions required to rework from a previous version or revision, if any.

# Manufacturing Assembly Instructions

* 1. **Parts required:**

***Section 2.1 should only be changed by changing the variables in the PCAMAP menu item. No other changes are to be made unless agreed upon by the NPIE team.***

* + 1. **General**
       1. Unless otherwise noted below, install all parts per the current revision of assembly drawing **60-105172-01** and bill of materials **73-102931-03**.
       2. Verify that the fab number of the bare PCB is **28-102746-01**. This information is normally located on the solder (bottom) side of the PCB. If this information is not correct, either you have the wrong PCB or this is not the correct assembly procedure. Do not proceed until you have the correct material and documentation. Unless otherwise instructed by Cisco, do not begin the assembly processing of this board unless all the components, called out on the BOM above, are present.
    2. **Part Changes Not in Schematic**
       1. NONE
    3. **Part Changes Not in BOM but on POI list**
       1. NONE

***Please note the Part Changes Not in BOM section 2.1.3 is only recommended to be used for parts without Cisco PNs that have no intention of ever being used in production. Parts not in the BOM have no procurement visibility and proper quantities must be supplied by Cisco to the CM for each build in which they are required. When ever possible, ALL parts should be CUP’d or ECO’d into a BOM. If during prototype development you are within the BOM Freeze Window before a proto build (typically 5 days) it is strongly recommended to specify any and all BOM changes in a Deviation – Lite. This provides the traceability required to identify BOM deviations. If you plan to use this Part Changes Not in BOM section, please get approval from your NPIE Manager.***

## Assembly Steps and Procedures:

***Any information that the CM needs to follow to insure higher yields or that will make the assembly easier is to be added to this subsection. All information in each subsection is to remain stand alone so that insertion or deletion of each subsection does not affect the others. Photos or screen captures should be used when possible to show complex descriptions. Each photo or screen capture is to be labeled with a figure number and referenced in the corresponding subsection.***

***Please reference EDCS***[***-605019 PCA Assembly Best Practices for assembly instructions and best practices***](http://wwwin-eng.cisco.com/BMS/Mfg/MFG_ENG/MTG/605019_PCA_Assembly_Best_Practices_And_Guidelines.doc) ***that can be incorporated into the PCAMAP assembly instructions when applicable.***

* + 1. **General**
       1. PWB flatness: Flatness should be verified on BGA package sites of 47.5mm and above per the requirements on the fabrication drawing. 10% of the boards per PCB lot should be tested. Any out of specification measurement would require a 100% sampling response prior to assembly (This measurement may be performed by the PWB supplier at the Contract Manufacturer).
       2. Minimum soldermask features: BGA package sites with 0.8 mm pitch and below need to be inspected for adequate soldermask dam (measured soldermask web width should be 3 mils minimum). The sampling plan should be per the Mil-STD-10 5D,AQL of 1% for normal inspection (Typi al PCB Lot sizes are 26-50).
       3. **LCCC’s:** Component stand-off height is critical. Stand-off height is a function of pad paste volume. The minimum stand-off height is >= 0.0015”. Optimal stand-off height is 0.0025”. Stencil apertures should be 1:1 to the PCB pad soldermask opening. Use a stencil thickness of 0.006”. All LCCC solder paste deposits must be measured (AOI/SVS) to insure that they are the same (within 10% of each other) to prevent significant component tilt after assembly.
       4. Post Soldering Heat Sink Installation
          1. With PCB backplane connectors facing away, and the front panel I/O connectors facing toward you, the air-flow direction is from FRONT TO BACK OR BACK TO FRONT.
          2. When installing adhesive-backed heat sinks, verify the fins are parallel to this airflow direction and the component surface is free of any contamination or solvents.
          3. For cross-cut fin heat sinks, make sure the wider gap is parallel to the air-flow direction.
       5. Ensure that all LEDs and connectors are installed flush with PCB surface and aligned straight with respect to their silkscreens. Pay particular attention to board edge connectors.
    2. **Label Placement**
       1. Refer to the Cisco specifications for labels and printing requirements found on the BOM for each label part number. DO NOT use the part number and revision from the drawing itself or from this assembly procedure. Label the bill of materials assembly number and revision in the PCA area provided per the assembly drawing. Note: CAD artwork specified label locations supersede locations specified in label specification documents. Contact the Cisco EPE if clarification is required for label placement.
    3. **Mechanical Assembly**
       1. Press in connectors should be mounted flush with the board surface and end caps used to protect exposed pins
       2. Connectors are press-fit please process after SMT reflow.
       3. For location SFP\_S0, SFP\_S1 AND SFP\_S2 MUST USE SAME VENDORS. NO MIXED IN VENDORS.
       4. For location QSFP\_Q0, QSFP\_Q1 AND QSFP\_Q2 MUST USE SAME VENDORS. NO MIXED IN VENDORS.
       5. It may be necessary to mask the screw mounting holes on the bottom side of the board. The holes are designed in order to minimize solder pickup. No solder is allowed on the screw mounting holes.
       6. All screws and standoffs should be tightened to required torque outlined in [95-5874-01](https://tools.cisco.com/emco/eco/ecm/home?module=GetDocuments&id=715600.pdf&OrgID=1)
       7. Follow assembly instructions outlined in 62-XXXX-01.
    4. **PCB and Assembly Defect Repair:**

***These notes are to be the same for all PCAs. If one needs to be added, the NPIE team needs to agree on the note and the wording.***

* + - 1. Unless otherwise noted, all jumpers (30 ga wire min) are to be installed on the component side of the board.
      2. Jumper connections are to be used as a reference for jumper wire end points only and do not define routing paths.
      3. All wires should be routed around ICs and tacked to the PCB using glue or tape at intervals of 1.5" or less. Wires should not touch IC legs or other component pins except at end points.
      4. All rework must meet or exceed latest revision of IPC-R-700 Class 2.
      5. If the Leffe board (CPN 73-101845-0X) in the system is replaced with a different board, follow 2.3.2 to reprogram the MAC’s for the management ports.

## Test Requirements

* + 1. X-ray shall be used (as a minimum requirement) to verify solder joints on all of the BGA packages present on the board. Additionally, (if Available) shall be performed on the board to ensure solder joint quality and bad component identification. For defects found using both tests, the board shall be fixed and the rework recorded by serial number and archived for future reference.
    2. Instruction for programming the MAC for the management ports on Leffe. Leffe needs two MAC's (1 for SFP, and 1 for RJ45 copper). Assign the first 2 MAC’s to Leffe. For service, rework and repair, to check and reprogram if the MAC’s on Leffe does not match with the first two MAC’s on Sumpin.

# Programming Instructions

* 1. Programmable Devices Data
     1. See Table 1 for the programmable data information. If the pre-programmed image in the devices is not the same as those listed in the table, then the images are to be updated to match those listed in the table.
     2. The files for the 17-level images can be found in Agile.

Table 1 - Programmable Data

|  |  |  |  |
| --- | --- | --- | --- |
| **Image Desc** | **Ref Des** | **Part Number** | **Filename** |
| MI\_FPGA | MIROM1 | 17-15887-04  16-1011779-07 | mi\_elysian\_v16\_auto.rpd |
| CPLD | CPLD1-CPLD3 | 17-13886-01  16-4342-01 | salt\_lake\_city\_imp\_0\_v2 |
| CPLD | CPLD4 | 17-14336-01  16-4342-01 | sumpin\_imp\_0\_v2 |
| PWR CONTROLLER | U1\_5 | 17-15181-02 15-103791-01 | 17-15181-02-00\_SD1\_6P1\_0P875.mic |
| POWER CONTROLLER | U1\_RTV1, U1\_TRV2 | 17-15781-01 15-103791-01 | 17-15781-01-00-pmbaddr-0x60-BV1+1.mic |

# SPROM Programming Instruction

* 1. Reference the XXX-PROM Programming Document used to program XXX-PROM.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Block #** | **Offset** | **Range** | | Block Size (Bytes) | |  |
| 1 | 0x0 | 0x0 – 0x9F | | 160 | |  |
| 2 | 0xA0 | 0xA0 – 0x106 | | 103 | |  |
| 3 | 0x107 | 0x107 – 0x14D | | 71 | |  |
|  |  |  | |  | |  |
| **Block # 1 - Common Block** |  |  | |  | |  |
| **Byte address** | | **item** | | **Value (decimal/hex)** | **comment** | |
| (hex) | (dec) |
| 0-1 | 0-1 | block signature | | 0xabab | 0xabab | |
| 2 | 2 | block version | | 3 | 3 | |
| 3 | 3 | block length | | 160 | 160 | |
| 4-5 | 4-5 | block checksum | |  | see section on checksum | |
| 6-7 | 6-7 | SPROM size | | 65535 | 65535 (64k Bytes) | |
| 8-9 | 8-9 | block count | | 3 |  | |
| 0A-0B | 10-11 | FRU major type | | 0x6002 | See FRU section | |
| 0C-0D | 12-13 | FRU minor type | | 0 | See FRU section | |
| 0E-21 | 14-33 | OEM string | | Cisco Systems, Inc. | Cisco Systems, Inc. | |
| 22-35 | 34-53 | product number | | **N9K-C93180YC-FX3** |  | |
| 36-49 | 54-73 | serial number | |  |  | |
| 4A-59 | 74-89 | part number | | 73-102931-03 | See PCA MAP | |
| 5A-5D | 90-93 | part revision | | A0 | See PCA MAP | |
| 5E-71 | 94-113 | mfg deviation | | 0 | used by manufacturing | |
| 72-73 | 114-115 | hw rev major | | 1 |  | |
| 74-75 | 116-117 | hw rev minor | | 0 |  | |
| 76-77 | 118-119 | mfg bits | | 0 |  | |
| 78-79 | 120-121 | eng bits | | 0x1 | bits[1:0]= 00 > not defined  bits[1:0]= 01 > Vishay  bits[1:0]= 10 > Onsemi  bits[1:0]= 11 > not defined | |
| 7A-89 | 122-137 | snmp OID | | 0.0.0.0.0.0.0.0 | Default = 0.0.0.0.0.0.0.0  (software will have its own table, no update plan) | |
| 8A-8B | 138-139 | power consumption | | -5008 | centiAmp, 601W (12V) | |
| 8C-8F | 140-143 | RMA failure code | | 0-0-0-0 | 0 | |
| 90-9B | 144-155 | CLEI code | | INMGF00CRF | Default = 12345678 | |
| 9C-9F | 156-159 | VID | | V06 | Version ID Default = V01 | |
|  |  |  | |  |  | |
| **Block #2 -** |  |  | |  |  | |
| **Byte offset** | | **item** | | **Value (decimal/hex)** | **comment** | |
| **(hex)** | **(dec)** | |  |
| 0-1 | 0-1 | | block signature | 0x6002 | 0x6002 | |
| 2 | 2 | | block version | 2 | 2 | |
| 3 | 3 | | block length | 103 | 103 | |
| 4-5 | 4-5 | | block checksum |  | see section on checksum | |
| 6-D | 6-13 | | feature bits | 0 |  | |
| E-15 | 14-21 | | hw changes bits | 0x1114 | Nibble 3 (new):  1 = new ASIC FW1201  Nibble2 (highlighted) 0= raw ZL30772 DPLL 1= preprogrammed ZL30772 DPLL  Nibble 1                                                  1 = Default   Nibble 0 4 = Default | |
| 16-17 | 22-23 | | card index | 21212 |  | |
| 18-1D | 24-29 | | MAC base |  | Auto-generated | |
| 1E-1F | 30-31 | | MAC length | 100 | 48 front SFP ports + 6\*4 (uplink breakout) + 12 (internal usage) + 16 (FC port channels and spares)= 100 MACs | |
| 20 | 32 | | EOBC connections | 0 |  | |
| 21 | 33 | | EPLD num | 0 |  | |
| 22-3F | 34-63 | | EPLD versions | 0 | uint16\*15 or uint8\*30 | |
| 40-4F | 64-79 | | Port info | 2-54;7-1 | type-num; type-num;... | |
| 50-51 | 80-81 | | SRAM size | 0 | in kB | |
| 52-61 | 82-97 | | 8 temp sensor info (major/minor) | 70/42 | 1. Intake temp sensor (inlet) | |
| 80/70 | 2. Exhaust temp sensor (outlet) | |
| 90/80 | 3. Broadwell-DE CPU | |
| -128/-128 | 4. Unused | |
| 110/100 | 5. CPU VRM | |
| 110/90 | 6. Sugarbowl/Homewood | |
| 120/110 | 7. Sugarbowl VRM | |
| |  | | --- | | -128/-128 | | N/A | |
| 62-63 | 98-99 | | max connector power | 5416 | centiAmp | |
| 64-65 | 100-101 | | cooling requirement | 100 | cfm, see Cooling Req Section | |
| 66 | 102 | | ambient temperature | 55 | degrees Celsius | |
|  |  | |  |  |  | |
| **Block #3 - Sensor Block** |  | |  |  |  | |
| **Byte offset** | | **item** | | **Value (decimal/hex)** | **comment** | |
| **(hex)** | **(dec)** |  | |
| 0-1 | 0-1 | block signature | | 0x6008 | 0x6008 | |
| 2 | 2 | block version | | 1 | 1 | |
| 3 | 3 | block length | | 71 | 71 | |
| 4-5 | 4-5 | block checksum | |  | see section on checksum | |
| 6 | 6 | number of valid sensors | | 0 | # of valid sensors in his block | |
| 7 - 46 | 7 - 70 | 32 temp sensor info (major/minor) | | -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | NA | |
| -128/-128 | Sensor instances 15 - 39 | |

# PCA Rework

No rework

# 6.0 References

6.1 EDCS-643205 PCAMAP Standardization Document

6.2 EDCS-605019 PCA Assembly Best Practices and Guidelines

6.3 EDCS-7000160 ECO Process & Tools Procedure

6.4 EDCS-7003900 Revision Version Policy

6.5 EDCS-7003340 BOM Structure Policy

6.6 EDCS-231946 Cisco UDI Compliance Specification

6.7 EDCS-231945 Unique Device Identifier (UDI) Policy

6.8 EDCS-7024110 CLEI Code Process